SIMPlugIN-LX45 User Manual

... a SIMPlugIN board® family member

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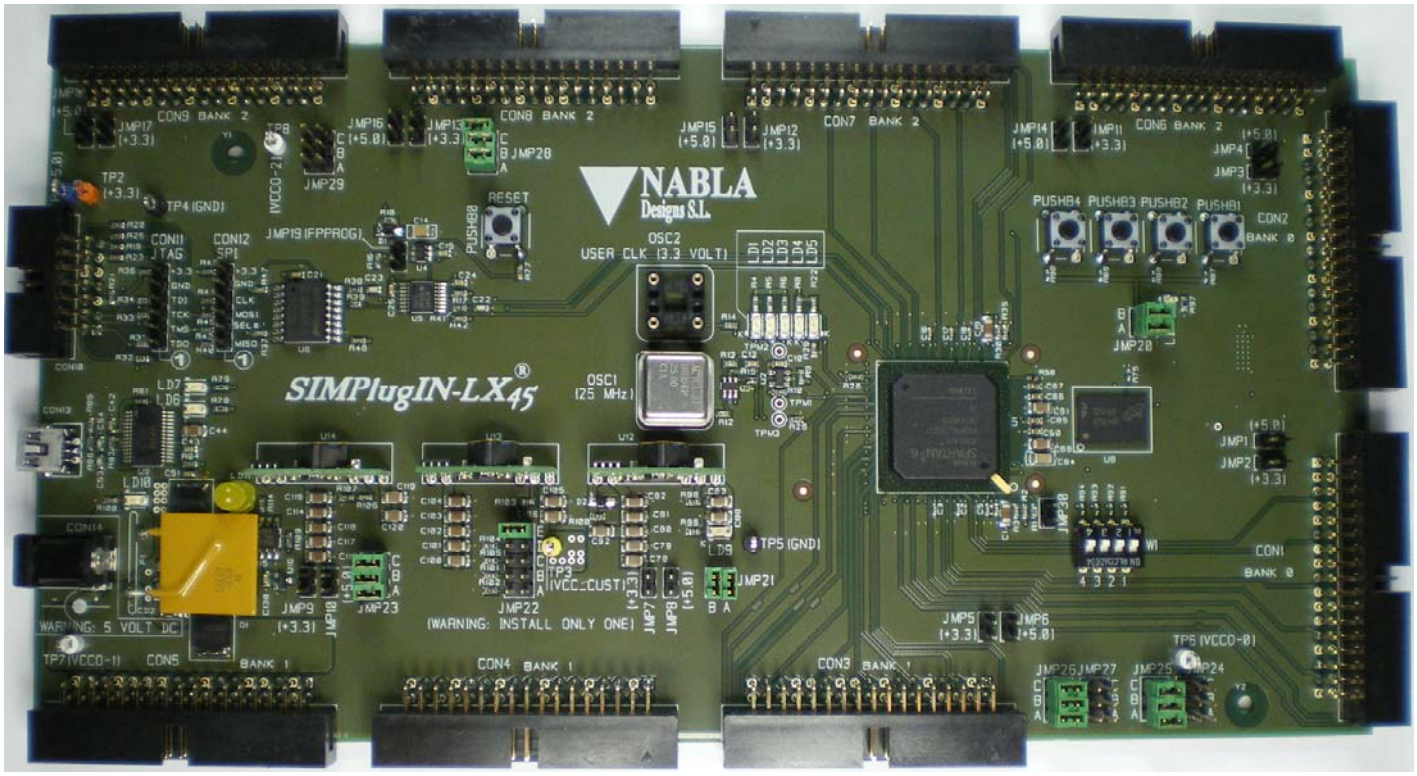
Date: September 13th 2011



REVISION HISTORY

0.1	First release
0.2	Corrected factory default jumper configuration

APENDICES

0) Introduction and references

This manual describes how to operate SIMPlugIN-LX45 board.

SIMPlugIN board is intended for engineers (engineering students too) that want to enjoy an easy to use and easy to expand FPGA developpment board.

This board provides on board the essential elements

- FPGA itself (in this case: Xilinx Spartan 6 model LX45 in BGA 484 package, 2 speed grade, Comercial temperature range)
- DDR2 memory; 64Mx16 (128 Mbytes), up to 300 MHz clock, 600 MHz data rate.
- SPI flash memory: 64Mbit (8 Mbyte) for fpga content (a little less than 2 Mbyte) plus 6 Mbyte extra of aditional storage (for instance for Microblaze embedded processor firmware)
- Power supply
- Console port (USB serial device)
- A few user leds and switches

In adition to these essential elements the board offers 9 connectors with 20 fpga pins each (**a total for 180 pins available to the user**).

The connectors are standard and easy to use:

- 0.10” (2.54 mm) pitch
- 2x17 right angle male header
- fully polarized

SIMPlugIN board® family offers many off the self boards that inmediately expand the capability of SIMPlugIN-LX45 board. At the date of writing this manual there are 8 models avialable of add-on boards:

- SIMPlugIN-VIDEO video DAC to be able to implement VGA video output.
- SIMPlugIN-ETHERNET 100 with 10/100 Ethernet phy chip.
- SIMPlugIN-USB with USB 2.0 (12 Mbit, full speed) device transceiver chip
- SIMPlugIN- SD with SD card slot
- SIMPlugIN- SERIAL 1 x RS232 plus 2 x RS485 (the three interfaces can be used simultaneously)
- SIMPlugIN-LED 20 x test point plus 20 x led (both red and green led for each test point)
- SIMPlugIN-DIGIT with 2 x hex display (7 segment display) + 4 micro switches
- SIMPlugIN-PROT prototyping board with perforated 0.10” grid and two sided plated holes

0.1) References

Note: from time to time companies modify their web pages. So, some of the detailed web link may be obsolete when you read the present document.

- Many documents are available in www.xilinx.com concerning Spartan 6 FPGA. In http://www.xilinx.com/support/documentation/spartan-6.htm there is comprehensive list of them.
- W971GG6JB DDR2 SDRAM data sheet Revision A06 in www.winbond.com
- W25Q64BV (64M-bit) Serial (SPI) Flash memory data sheet Revision E in www.winbond.com
- Male, 2x17 pin connector (on SIMPlugIN-LX45 board) model 75867-106LF. See 75867 family data sheet Rev:AM Dec 1 6 , 2 0 1 0 in www.fciconnect.com
- Female 2x17 pin connector (on all SIMPlugIN add-on boards) model SFH11-PBPC-D17-RA-BK. See data sheet in www.sullinscorp.com
- FT232RL usb-serial chip. See datasheet and download software drivers (for Windows, Linux, Mac,…) in www.ftdichip.com
- 24AA02E48T eeprom with I2C interface and unique serial number. See data sheet in www.microchip.com

1) General description

1.1) Overall block diagram

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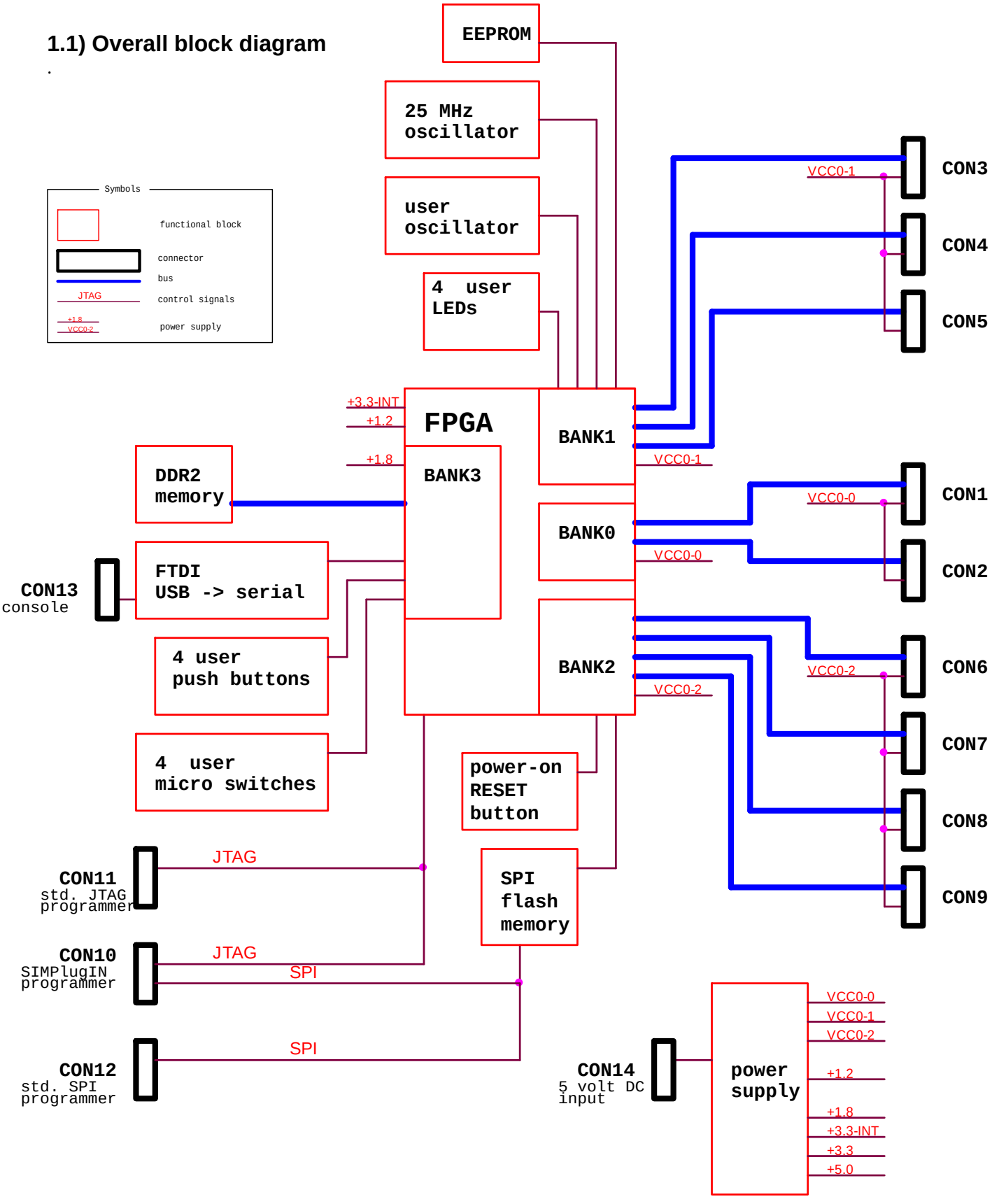
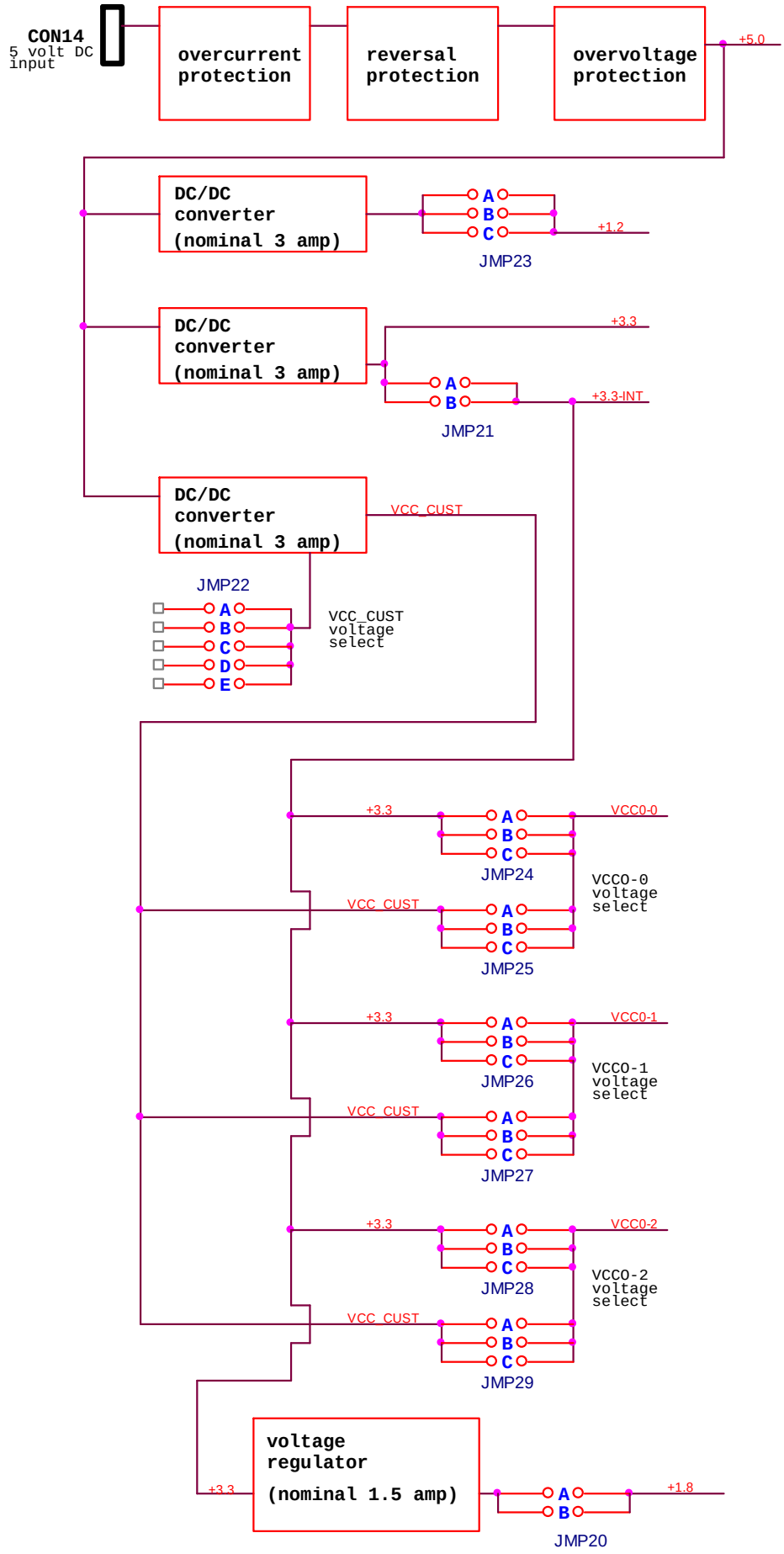


1.2) Power supply block diagram



Some jumpers should always be populated (in ALL its positions) in normal operation. Their function is to allow the user to open the circuit and so be able to put in series ammeter(s) to monitor the current(s) of each power supply.
:

JMP23 to monitor +1.2 power supply (the one used by FPGA core)
JMP20 to monitor +1.8 power supply (used by DDR2 and bank 3 of FPGA chip)
JMP21 to monitor +3.3-INT (used to power VCCAUX of FPGA chip AND to feed the linear voltage regulator that generates +1.8 power supply

Notes:

a) In adition of DDR2 and bank 3 of FPGA, +1.8 supplies a little current to FTDI chip and some pullups (see page 4 of the schematics).
b) [current used by VCCAUX] = [current measured in JMP21] – [current measured in JMP20]

The rest of the jumpers shown in the above figure are configuration jumpers

JMP22 configures the voltage of VCC_CUST

- position A populated, all others not populated: 1.2 volt
- position B populated, all others not populated: 1.5 volt
- position C populated, all others not populated: 1.8 volt
- position D populated, all others not populated: 2.5 volt
- position E populated, all others not populated: 3.3 volt

Note: all other combinations are not harmful but are not usual. For example:

- all positions not populated: 0,75 volt (too low)
- position C and D both populated, all other not populated: 2.64 volt (not standard)

JMP24 and JMP25 configure VCCO-0
FPGA bank 0
Asociated user connectors: CON1 and CON2

JMP24	JMP25	voltage
fully populated	completely NOT populated	VCC_CUST
completely NOT populated	fully populated	+3.3
All other combinations		ILEGAL, **dangerous**

DANGER !! some illegal icombinations could damage the board and/or add-on boards pluged into ANY of user connector, **even corresponding to OTHER banks**.

JMP26 and JMP27 configure VCCO-1
FPGA bank 1
Asociated user connectors: CON3 , CON4 and CON5

JMP26	JMP27	voltage
fully populated	completely NOT populated	VCC_CUST
completely NOT populated	fully populated	+3.3
All other combinations		ILEGAL, **dangerous**

DANGER !! some illegal icombinations could damage the board and/or add-on boards pluged into ANY of user connector, **even corresponding to OTHER banks**.

JMP28 and JMP29 configure VCCO-2
FPGA bank 1
Asociated user connectors: CON6 , CON7 , CON8 and CON9

JMP28	JMP29	voltage
fully populated	completely NOT populated	VCC_CUST
completely NOT populated	fully populated	+3.3
All other combinations		ILEGAL, **dangerous**

DANGER !! some illegal icombinations could damage the board and/or add-on boards pluged into ANY of user connector, **even corresponding to OTHER banks**.

1.2.1) Power Input voltage and protections

The board must be powered with 5 volt DC with +/- 5% tolerance. A maximun current of 3 AMP (so 15 wats) is specified.

A cable is provided to power the board from a laboratory power supply. This cable is not standard but is composed of standard componentes:
- 1 unit of cable assemblly with power jack.
- 1 unit of red PLUG BANANA.
- 1 unit of black PLUG BANANA.

To power the board from AC mains (if you do not have laboratory power supply) use a wall power supply unit with 5 volt DC , 3 amp. Notice that such a wall power unit is optional and must be purchased separatedly.

Many protections are provided

- **Over current**:
  - nominal 3 amp resettable fusible proteccts 5 volt DC input
  - +1.8 is current limited (around 2.4 amp) by its voltage regulator. Also it thermally protects itself.
  - +1.2 , +3.3 (that includes +3.3-INT) and VCC_CUST are independtly current limited by its respective voltage regulator (around 6 amp). Also each is independently thermally protected.
- **Voltage reversal**: the input will tolerate a reversed voltage down to minus 17 volt. Any voltage bellow that (either continous or temporary peak) will damage the board
- **Overvoltage**: the input will tolerate up to 17 volt of DC. Any voltage about that (either continous or temporary peak) will damage the board.

Reverse voltage symptom: the board will not be internally powered a not a single LED will be lit.

Overvoltage symtom: LD11 will be lit, all the others will not. Notice that LD11 is the only yellow led in the board, also is the only 5 mm through hole led.

BE CAREFUL, **even with those protections the board will not survive a "masive" abuse like connecting it directly to the AC mains (even the relatively "mild" 100 AC volt mains in U.S.A)**
MORE: you clearly risk FIRE if you do it.

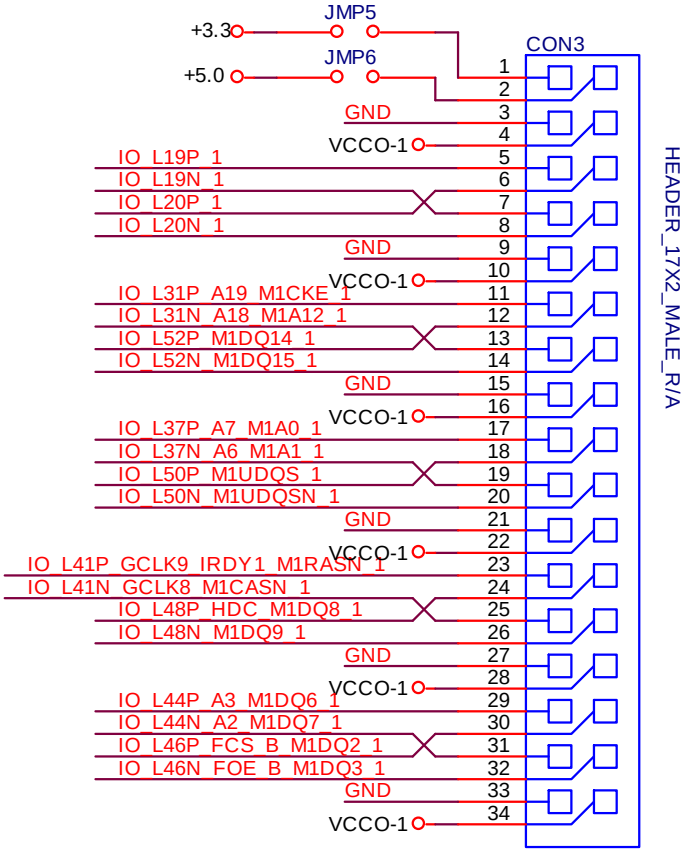
1.3) User connectors

Each of the nine (CON1, CON2,…CON9) user connectors provides 20 FPGA I/O pins plus 3 different power supplies:

- VCCO correspondiing to its asociated bank
- 3.3 volt
- 5.0 volt

DANGER !! if the user uses 5.0 volt. in his or her custom add-on board then care must be taken that any of the 20 FPGA pins does NOT receive more than 3.3 volt since FPGA pins tolerate without problem 3.3 volt (even if the bank is powered by a much lower voltage like 1.8 volt or 1.5 volt) but will NOT tolerate higher than 4 volt (the FPGA chip would get permanently damaged !!). For a working example see schematics of SIMPlugIN- SERIAL board that uses 5 volt but does not send any 5 volt signal back to FPGA pins.

With very minor exceptions (see next point bellow) the pins in the 9 user connector are distributed as shown in the following figuere



See detailed complete pin-out in 2.6) point in this documents.

Notice:

- power (VCCO-? , +3.3 and +5.0) are always in the same pins in all the connectors (where "?" in VCCO-? Is 0, 1, or 2 for FPGA bank 0, 1, 2, respectively)
- pin 23 and pin 25 are always a pair of global clocks (can be used as a differencial pair or as two separated single ended clocks).
- two connectors, CON1 and CON2 have one aditional pair of global clocks
- the 20 pins are grouped in 10 pairs that follow paired pins of FPGA (with only one single exception in CON2, see next point bellow). The two tracks, negative and positive, of each pair have PCB tracks that are carefully matched lenghts (notice different pairs have different lenghts, that is, the pairs are matched within themselves but NOT with respect to other pairs).
- +3.3 and +5.0 power lines are fed to the connector through jumpers. Remove these jumpers unless you are really using this power supplies in your custom add-on board.

1.4) Exceptions in user connector uniformity

Each of the nine (CON1, CON2,…CON9) are very similar except the following differences:

- CON2 , pins 6 and 8 do NOT correspond to a pair of FPGA pins.
- CON1 and CON2 have an aditional pair of global clocks.
- CON1 and CON2 are connected to FPGA bank 0 and powered by VCCO-0 (as bank 0 itself)
- CON3 , CON4 and CON5 are connected to FPGA bank 1 and powered by VCCO-1 (as the bank 1 itself)
- CON6 , CON7, CON8 and CON9 are connected to FPGA bank 2 and powered by VCCO-2 (as the bank 2 itself)

1.5) VREF for FPGA banks

Each FPGA bank 0,1,2 have a voltage divider (implemented with two 100 ohm resistors) bypassed with capacitors that feeds all the VREF pins of each bank with its VCC0-? divided by two (where "?" is 0,1,2) . That allows the user to select for each pin all I/O standard except HSTL_III and HSTL_III_18 (the only two I/O standard that require VREF different to VCCO / 2). See Xilinx documents "Spartan-6 FPGA Data Sheet: DC and Switching Characteristics" and "Spartan-6 FPGA SelectIO Resources User Guide"

1.6) Oscillators

The board ships with a 25 MHz oscillator in OSC1 position. Since it is on socket the user can easily change it but it must be taken into account that:

- some of the FPGA examples provided suposse that this oscillator is 25 MHz if you change the frequency the behaviour of these examples (for instance, the one that exercises the USB device interface) could stop working (or will need a change in the example source code).

The other oscillator (user oscillator in OSC2 position) is an empty socket available to the user.

Note: the oscillator installed must be 3.3 volt , CMOS type. Notice (see schematic) that the oscillator is allways powered by 3.3 volt. The ouput of the oscillator is fed to the FPGA thorough buffers that act as level translators into whatever power is selected for bank 1.

1.7) EEPROM

EEPROM is implemented with 24AA02E48T from Microchip. The interface with this eeprom is I2C. This eeprom provides a unique, read-only, number and identfies your board. Do not change this chip since that action would void the warranty. The write/read part of the eeprom is fully available to the user.

1.8) User LEDs, pushbuttons and microswtiches

The boad provides 4 leds, 4 pushbuttons and an one microswitch with 4 position.

1.9) Power-on reset

The board provides one pushbutton , PUSHB0, (independent of the four user pushbuttons mentioned above). When pressed this the signal RESET_POW_ON will be activated for about 100 msec after releasing PUSHB0. This will allow to implement a user "power on reset.

1.10) SPI flash memory

The board provides SPI flash, 64 Mbit (8 Mbyte) memory that will contain FPGA configuration (a little less than 2 Mbyte); that leaves 6 Mbytes for user data (for instance code and data for a Microblaze embeded processor).

It is implement using W25Q64BVSFIG Winbond chip.

The chip is always powered by 3.3 volt. A level translator chip copes with actual power of bank 2.

So, regardless of the power level used by bank 2 (for instance, 1.8 volt) the SPI flash chip will always work at 3.3 volt. Same will happen with external SPI programmer (either SIMPlugIN programmer or any standar SPI programmer): the working voltage will be 3.3 volt.

The SPI memory can be programmed by an standard SPI programmer (using CON12) or SIMPlugIN programmer (using CON10).

1.11) FTDI USB -> serial chip

The FT232RL FTDI chip interfaces USB (PC side) to serial (FPGA side) and provides a serial interface to FPGA (for instance for a serial console).

Even if FPGA is not configured, if the board is powered when you connect (using standar USB A – mini USB cable) the board to the PC the FTDI should be recognized and a new COM port (for instance COM7) should appear in your PC. If it is not recognized then you should download software driver for your operating system (e.g. Windows 7 or Linux) for FT232R chip in www.ftdichip.com.

The signals provided are:

- FPGA-TxD (output from FPGA, input to FTDI RxD pin)
- FPGA-RxD (input to FPGA, output from FTDI TxD pin)
- FPGA-RTS# (active low, output from FPGA, input to FTDI CTS# pin)
- FPGA-CTS# (active low, input to FPGA, output from FTDI RTS# pin)

FTDI pin name	FTDI pin number	signal	FPGA ball name	FPGA ball number
RTS#	3	FPGA-CTS#	IO_L25P_3	M6
CTS#	11	FPGA-RTS#	IO_L25N_3	L6
TxD	1	FPGA-RXD	IO_L24P_3	R4
RxD	5	FPGA-TXD	IO_L24N_3	P4

1.12) DDR2 memory

Provided by one W971GG6JB Winbond chip with 64M x 16 (128 Mbyte) DDR2 SDRAM memory chip.

Notice when devoloping your FPGA (using Xilinx ISE tools) and implement memory you should enter DDR2 memory and then select as “model” Micron MT47H64M16XX-25 that is Micron memory exact to W971GG6JB Winbond.

The memory can be operated up to 300 MHz clock (600MHz data rate).

1.13) JTAG interface

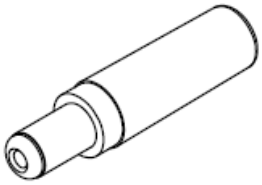
There are two connector to plug a JTAG programmer. CON11 for standard JTAG programmer and CON10 for SIMPlugIN JTAG/SPI programmer.

In both cases the programmer will “see” 3.3 volt working voltage (regardless of the actual voltage configured for bank 2).

2) Connectors

2.1) CON14 , power input

The board should be powered with 5 volt DC with female power plug with 2.1mm Inner Diamter and 5.5mm Outer diameter. Since the expected current for the board is 3 Amp then the connector should be rated at 5 Amp.

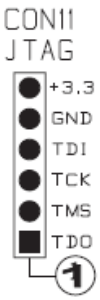


CON14 pin out

Outer contact	0 volt
Inner contact	+5 vol DC

2.2) CON11, JTAG programming for standard programmers

6x1 male header, 0.10" (2.54 mm) pitch is provided.



CON11 pin out

1	TDO
2	TMS
3	TCK
4	TDI
5	GND
6	3.3 volt

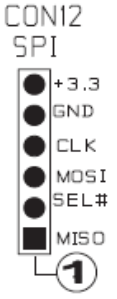
Pin 1 is clearly marked as well as the function of each pin

CAUCTION: carefully verify that the connection that you make match the stated functionality of each pin. Except for GND all the pins have series resistor (330 ohm for +3.3 and 100 ohm for the rest). This series resistor do not normally interfere with JTAG programmer and are reasonable protection if the conections are missplaced. If the connections are OK and **If you have problems with your JTAG programmer try reducing the programming clock frequency.**

Notice: due to the 330 ohm series resistor in pin 6, this pin can NOT power supply the JTAG programmer.

2.3) CON12, SPI programming for standard programmers

6x1 male header, 0.10" (2.54 mm) pitch is provided.



CON12 pin out

1	MISO (output fron the board, input to the programmer)
2	SEL# (chp select, input to the board)
3	MOSI (input to the board)
4	CLK (output from the programmer)
5	GND
6	3.3 volt

Pin 1 is clearly marked as well as the function of each pin

CAUCTION: carefully verify that the connection that you make match the stated functionality of each pin. Except for GND all the pins have series resistor (330 ohm for +3.3 and 100 ohm for the rest). This series resistor do not normally interfere with SPI programmer and are reasonable protection if the conections are missplaced.. If the connections are OK and **If you have problems with your SPI programmer try reducing the programming clock frequency.**
Notice: due to the 330 ohm series resistor in pin 6, this pin can NOT power supply the SPI programmer.

IMPORTANT: **while using the external standard SPI programmer JMP19 must be populated** this will force the FPGA SPI related pins to HiZ and so the SPI could be driven by external programmer. Remove that jumper after SPI programming to allow normal operation.

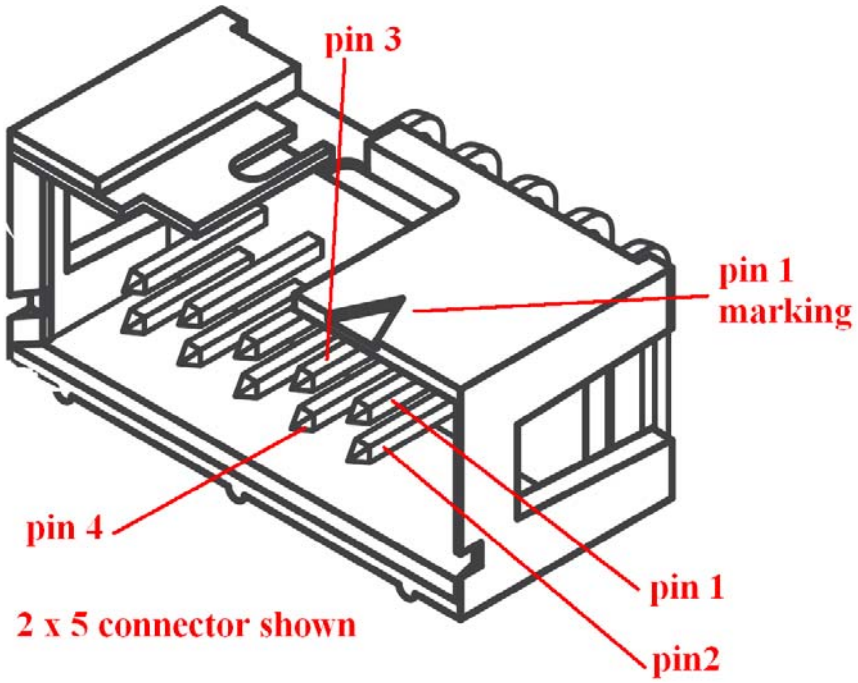
2.4) CON10, SPI and JTAG programming for SIMPlugIN programmer

7 x 2 male header, right angle, shrouded- Standard pin numbering (see drawing bellow).

Specific connector for SIMPlugIN programmer (SPI + JTAG programmer)

CON10 pin out

1	TDO
2	TMS
3	TDI
4	TCK
5	3.3 volt
6	INIT
7	DONE
8	PROG
9	5.0 volt
10	GND
11	MISO
12	CLK
13	SEL#
14	MOSI

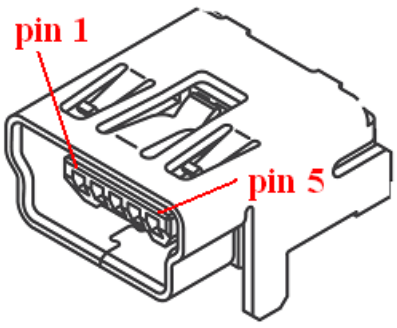


2.5) CON13, mini USB

Standard mini-B , USB, receptacle, right angle, through hole

CON13 pin out

1	+5.0
2	DAT-
3	DAT+
4	ID (NOT connected)
5	GND



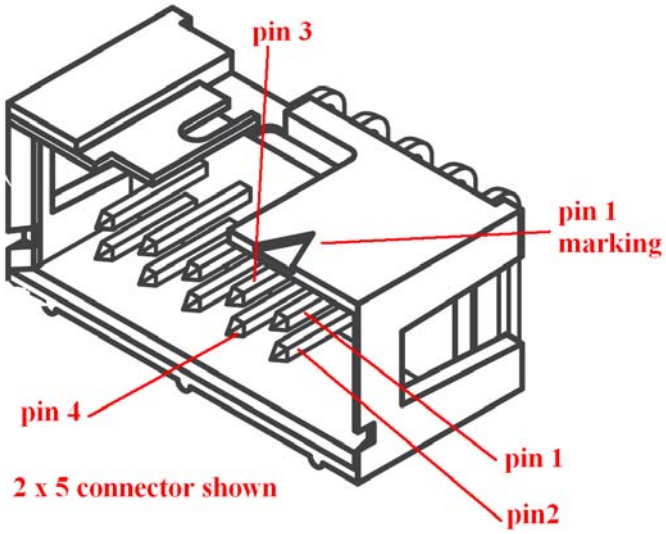
The usb connects to a USB -> serial chip from FTDI (FT232R)

2.6) CON1, CON2,…, CON9: User connectors

17 x 2 male header, right angle, shrouded- Standard pin numbering (see drawing in bellow).

NOTICE that in all user connectors pins that connect to FPGA balls are routed in PCB as a pair and always goes to two paired FPGA pins. The pairs are:

5 and 7
6 and 8
11 and 13
12 and 14
17 and 19
18 and 20
23 and 25
24 and 26
29 and 31
30 and 32



ONLY exception: CON2, pins 6 and 8 do NOT make a pair.

All connectors provides 2 paired global clock. Aditionally CON1 and CON2 provides 2 aditional paired global clocks.

Recommended mating conector (to be used in add-on boards) Sullins Connector Solutions p/n SFH11-PBPC-D17-RA-BK. This connector is polarized and keyed so it is imposible to missplace it when pluging it into the user connectors.

2.6.1) BANK 0 user connectors

CON1 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-0	-
5	IO_L4P_0	B6
6	IO_L64P_SCP5_0	C17
7	IO_L4N_0	A6
8	IO_L64N_SCP4_0	A17
9	GND	-
10	VCCO-0	-
11	IO_L6P_0	B8
12	IO_L51P_0	C15
13	IO_L6N_0	A8
14	IO_L51N_0	A15
15	GND	-
16	VCCO-0	-
17	IO_L34P_**GCLK19**_0	B10
18	IO_L33P_0	D10
19	IO_L34N_**GCLK18**_0	A10
20	IO_L33N_0	C10
21	GND	-
22	VCCO-0	-
23	IO_L37P_GCLK13_0	B12
24	IO_L65P_SCP3_0	B18
25	IO_L37N_GCLK12_0	A12
26	IO_L65N_SCP2_0	A18
27	GND	-
28	VCCO-0	-
29	IO_L50P_0	B14
30	IO_L63P_SCP7_0	B16
31	IO_L50N_0	A14
32	IO_L63N_SCP6_0	A16
33	GND	-
34	VCCO-0	-

CON2 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-0	-
5	IO_L3P_0	D6
6	**IO_L62P_0**	D15
7	IO_L3N_0	C6
8	**IO_L38P_0**	C13
9	GND	-
10	VCCO-0	-
11	IO_L7P_0	D9
12	IO_L49P_0	D14
13	IO_L7N_0	C8
14	IO_L49N_0	C14
15	GND	-
16	VCCO-0	-
17	IO_L36P_**GCLK15**_0	D11
18	IO_L32P_0	D7
19	IO_L36N_**GCLK14**_0	C12
20	IO_L32N_0	D8
21	GND	-
22	VCCO-0	-
23	IO_L35P_GCLK17_0	C11
24	IO_L5P_0	C7
25	IO_L35N_GCLK16_0	A11
26	IO_L5N_0	A7
27	GND	-
28	VCCO-0	-
29	IO_L66P_SCP1_0	E16
30	IO_L2P_0	C5
31	IO_L66N_SCP0_0	D17
32	IO_L2N_0	A5
33	GND	-
34	VCCO-0	-

Notes:

- CON2 pins 6 and 8 do NOT correspond a pair of FPGA balls. These are the only exception in all 9 user connectors
- Pins 23 and 25 are paired global clocks in all 9 user connectors.
- CON1 and CON2 are exceptional since both have and aditional pair of global clocks in pins 17 and 19

2.6.2) BANK 1 user connectors

CON3 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-1	-
5	IO_L19P_1	B21
6	IO_L20P_1	A20
7	IO_L19N_1	B22
8	IO_L20N_1	A21
9	GND	-
10	VCCO-1	-
11	IO_L31P_A19_M1CKE_1	D21
12	IO_L52P_M1DQ14_1	V21
13	IO_L31N_A18_M1A12_1	D22
14	IO_L52N_M1DQ15_1	V22
15	GND	-
16	VCCO-1	-
17	IO_L37P_A7_M1A0_1	F21
18	IO_L50P_M1UDQS_1	T21
19	IO_L37N_A6_M1A1_1	F22
20	IO_L50N_M1UDQSN_1	T22
21	GND	-
22	VCCO-1	-
23	IO_L41P_GCLK9_IRDY1_M1RASN_1	H21
24	IO_L48P_HDC_M1DQ8_1	P21
25	IO_L41N_GCLK8_M1CASN_1	H22
26	IO_L48N_M1DQ9_1	P22
27	GND	-
28	VCCO-1	-
29	IO_L44P_A3_M1DQ6_1	K21
30	IO_L46P_FCS_B_M1DQ2_1	M21
31	IO_L44N_A2_M1DQ7_1	K22
32	IO_L46N_FOE_B_M1DQ3_1	M22
33	GND	-
34	VCCO-1	-

CON4 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-1	-
5	IO_L32P_A17_M1A8_1	C20
6	IO_L29P_A23_M1A13_1	D19
7	IO_L32N_A16_M1A9_1	C22
8	IO_L29N_A22_M1A14_1	D20
9	GND	-
10	VCCO-1	-
11	IO_L35P_A11_M1A7_1	E20
12	IO_L30P_A21_M1RESET_1	F18
13	IO_L35N_A10_M1A2_1	E22
14	IO_L30N_A20_M1A11_1	F19
15	GND	-
16	VCCO-1	-
17	IO_L39P_M1A3_1	G20
18	IO_L51P_M1DQ12_1	U20
19	IO_L39N_M1ODT_1	G22
20	IO_L51N_M1DQ13_1	U22
21	GND	-
22	VCCO-1	-
23	IO_L43P_GCLK5_M1DQ4_1	J20
24	IO_L49P_M1DQ10_1	R20
25	IO_L43N_GCLK4_M1DQ5_1	J22
26	IO_L49N_M1DQ11_1	R22
27	GND	-
28	VCCO-1	-
29	IO_L45P_A1_M1LDQS_1	L20
30	IO_L47P_FWE_B_M1DQ0_1	N20
31	IO_L45N_A0_M1LDQSN_1	L22
32	IO_L47N_LDC_M1DQ1_1	N22
33	GND	-
34	VCCO-1	-

CON5 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-1	-
5	IO_L10P_1	F16
6	IO_L33P_A15_M1A10_1	G19
7	IO_L10N_1	F17
8	IO_L33N_A14_M1A4_1	F20
9	GND	-
10	VCCO-1	-
11	IO_L9P_1	G16
12	IO_L38P_A5_M1CLK_1	H20
13	IO_L9N_1	G17
14	IO_L38N_A4_M1CLKN_1	J19
15	GND	-
16	VCCO-1	-
17	IO_L34P_A13_M1WE_1	H19
18	IO_L60P_1	W20
19	IO_L34N_A12_M1BA2_1	H18
20	IO_L60N_1	W22
21	GND	-
22	VCCO-1	-
23	IO_L40P_GCLK11_M1A5_1	K20
24	IO_L58P_1	M16
25	IO_L40N_GCLK10_M1A6_1	K19
26	IO_L58N_1	L15
27	GND	-
28	VCCO-1	-
29	IO_L59P_1	P19
30	IO_L21P_1	K16
31	IO_L59N_1	P20
32	IO_L21N_1	J16
33	GND	-
34	VCCO-1	-

2.6.3) BANK 2 user connectors

CON6 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-2	-
5	IO_L53P_2	W6
6	IO_L47P_2	W9
7	IO_L53N_2	Y6
8	IO_L47N_2	Y8
9	GND	-
10	VCCO-2	-
11	IO_L54P_2	Y5
12	IO_L43P_2	Y9
13	IO_L54N_2	AB5
14	IO_L43N_2	AB9
15	GND	-
16	VCCO-2	-
17	IO_L62P_D5_2	W4
18	IO_L44P_2	W10
19	IO_L62N_D6_2	Y4
20	IO_L44N_2	Y10
21	GND	-
22	VCCO-2	-
23	IO_L30P_GCLK1_D13_2	Y13
24	IO_L20P_2	W14
25	IO_L30N_GCLK0_USERCCLK_2	AB13
26	IO_L20N_2	Y14
27	GND	-
28	VCCO-2	-
29	IO_L58P_2	Y3
30	IO_L21P_2	Y15
31	IO_L58N_2	AB3
32	IO_L21N_2	AB15
33	GND	-
34	VCCO-2	-

CON7 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-2	-
5	IO_L15P_2	Y17
6	IO_L6P_2	W18
7	IO_L15N_2	AB17
8	IO_L6N_2	Y18
9	GND	-
10	VCCO-2	-
11	IO_L14P_D11_2	AA18
12	IO_L5P_2	Y19
13	IO_L14N_D12_2	AB18
14	IO_L5N_2	AB19
15	GND	-
16	VCCO-2	-
17	IO_L19P_2	AA16
18	IO_L64P_D8_2	AA2
19	IO_L19N_2	AB16
20	IO_L64N_D9_2	AB2
21	GND	-
22	VCCO-2	-
23	IO_L31P_GCLK31_D14_2	AA12
24	IO_L57P_2	AA4
25	IO_L31N_GCLK30_D15_2	AB12
26	IO_L57N_2	AB4
27	GND	-
28	VCCO-2	-
29	IO_L45P_2	AA8
30	IO_L49P_D3_2	AA6
31	IO_L45N_2	AB8
32	IO_L49N_D4_2	AB6
33	GND	-
34	VCCO-2	-

CON8 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-2	-
5	IO_L11P_2	V17
6	IO_L9P_2	V19
7	IO_L11N_2	W17
8	IO_L9N_2	V18
9	GND	-
10	VCCO-2	-
11	IO_L17P_2	Y16
12	IO_L7P_2	T16
13	IO_L17N_2	W15
14	IO_L7N_2	T15
15	GND	-
16	VCCO-2	-
17	IO_L18P_2	V13
18	IO_L10P_2	R16
19	IO_L18N_2	W13
20	IO_L10N_2	R15
21	GND	-
22	VCCO-2	-
23	IO_L32P_GCLK29_2	Y11
24	IO_L63P_2	U6
25	IO_L32N_GCLK28_2	AB11
26	IO_L63N_2	V5
27	GND	-
28	VCCO-2	-
29	IO_L42P_2	V11
30	IO_L46P_2	W8
31	IO_L42N_2	W11
32	IO_L46N_2	V7
33	GND	-
34	VCCO-2	-

CON9 pin	FPGA pin name or power pin	FPGA ball number
1	3.3 volt	-
2	5.0 volt	-
3	GND	-
4	VCCO-2	-
5	IO_L50P_2	U9
6	IO_L40P_2	R11
7	IO_L50N_2	V9
8	IO_L40N_2	T11
9	GND	-
10	VCCO-2	-
11	IO_L59P_2	R9
12	IO_L8P_2	U17
13	IO_L59N_2	R8
14	IO_L8N_2	U16
15	GND	-
16	VCCO-2	-
17	IO_L22P_2	T12
18	IO_L23P_2	T14
19	IO_L22N_2	U12
20	IO_L23N_2	R13
21	GND	-
22	VCCO-2	-
23	IO_L29P_GCLK3_2	W12
24	IO_L60P_2	T7
25	IO_L29N_GCLK2_2	Y12
26	IO_L60N_2	R7
27	GND	-
28	VCCO-2	-
29	IO_L52P_2	T10
30	IO_L51P_2	T8
31	IO_L52N_2	U10
32	IO_L51N_2	U8
33	GND	-
34	VCCO-2	-

3) Configuration jumpers

3.1) Power supply configuration

Before proceding, please, REVIEW the following points:
- 1.2) Power supply block diagram
- 1.3) User connectors

DEFAULT jumper configuration

JMP20	Fully populated	SPECIAL: remove and substitute for ammeter to monitor +1.8 current
JMP21	Fully populated	SPECIAL: remove and substitute for ammeter to monitor +3.3-INT current
JMP22	Only C position populatted	To configure **VCC_CUST to 1.8 volt**
JMP23	Fully populated	SPECIAL: remove and substitute for ammeter to monitor +1.2 current
JMP24	Completely unpopulated	VCCO-0 (power supply for FPGA **bank 0 and its asociated connectors**
JMP25	Fully populated	**CON1 and CON2) configured to VCC_CUST**
JMP26	Fully populated	VCCO-1 (power supply for FPGA bank 1 and its asociated connectors
JMP27	Completely unpopulated	CON3, CON4 and CON5) configured to 3.3 volt
JMP28	Fully populated	VCCO-2 (power supply for FPGA bank 2 and its asociated connectors
JMP29	Completely unpopulated	CON6, CON7, CON8 and CON9) configured to 3.3 volt
JMP2	unpopulated	3.3 volt available in CON1
JMP1	unpopulated	5.0 volt available in CON1
JMP3	unpopulated	3.3 volt available in CON2
JMP4	unpopulated	5.0 volt available in CON2
JMP5	unpopulated	3.3 volt available in CON3
JMP6	unpopulated	5.0 volt available in CON3
JMP7	unpopulated	3.3 volt available in CON4
JMP8	unpopulated	5.0 volt available in CON4
JMP9	unpopulated	3.3 volt available in CON5
JMP10	unpopulated	5.0 volt available in CON5
JMP11	unpopulated	3.3 volt available in CON6
JMP14	unpopulated	5.0 volt available in CON6
JMP12	unpopulated	3.3 volt available in CON7
JMP15	unpopulated	5.0 volt available in CON7
JMP13	unpopulated	3.3 volt available in CON8
JMP16	unpopulated	5.0 volt available in CON8
JMP17	unpopulated	3.3 volt available in CON9
JMP18	unpopulated	5.0 volt available in CON9

NOTE-1: JMP22, JMP24 and JMP25 are configured so as to provide 1.8 volt to BAK0. The reason is that that bank is the default one for SIMPlugIN-VIDEO board that works ONLY with 1.8 volt. If that is not your case then configure BANK0 supply as needed.
NOTE-2: JMP1, JMP2,…., JMP18 are unpopulated but a female jumper is provided but installed so as NOT to short the tow pins of the jumper.

3.2) Other configuration jumpers

JMP30
- when populated pulls to low FPGA HSWAP pin (when this pin is low it enables I/O pullups before and during configuration)
- default: NOT populated

JMP19
- when populated forces the FPGA into programming mode and so it put all its pins en HiZ (with or without internal FPGA pullups depending on the state of HSWAP pin (see JMP30).
- Default: NOT populated

NOTES
- While using an SPI standard programmer it is necessary to install JMP19; that way the FPGA will relase these pins to the external programmer. Remove after programming is done to allow normal operation.
- That is not necessary when using SIMPlugIN programmers
- Momentary installation of JMP19 will force reloading of the FPGA.

4) LEDs, pushbuttons, microswitches, testpoints and oscillators

4.1) LEDs

4.1.1) User LEDS

There are 4 red LEDs available to the user. All are active low (lit when corresponding signal is low).

IMPORTANT: since the leds are supplied with fixed 3.3 volt (independent fo the voltage selected to supply bank2) then the LEDS must be managed as

Led ON: put the corresponding signal to low
LED OFF put the corresponding signal HiZ

LED	signal	Asociated FPGA ball name	Asociated ball number
LED1	LED0#	IO_L72P_1	P17
LED2	LED1#	IO_L71N_1	M18
LED3	LED2#	IO_L71P_1	M17
LED4	LED3#	IO_L70N_1	V20

4.1.2) Other LEDs

LD5 , green, will be ON after FPGA has finished configuration (from JTAG programmer or from on board SPI memory)

LD6 , green, will blink when there is activity in TX line of FTDI chip.
LD7 , green, will blink when there is activity in RX line of FTDI chip.

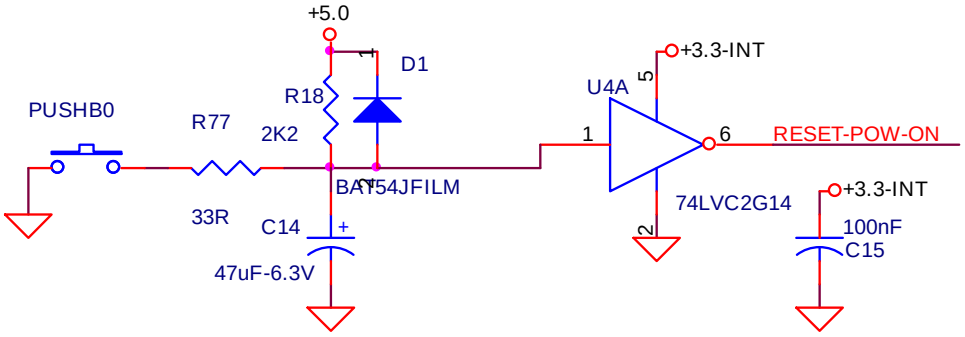
LD8 , green, will be ON when +1.8 volt is active
LD9 , green, will be ON when +3.3 volt is active
LD10 , green, will be ON when +5.0 volt is active

LD11, YELLOW, 5 mm. When ON it indicates OVERVOLTAGE in board power supply input. **DISCONNECT INMMEDIATELY** the power to the board and find out why the intended voltage is not 5 volt DC +/- 5% as it should.be.

4.2) Pushbuttons

4.2.1) PUSHB0

Its control circuits is



When pressed signal RESET-POW-ON is activated (high). When released R18 – C14 network maintains activation for around 100 msec. Note RESET-POW-ON correspondon to FPGA ball name IO_L4P_2, ball number T18.

IMPORTANT: when the board is powered up a 100ms pulse of RESET-POW-ON is generated but due to the time needed for FPGA configuration is most likely than when FPGA has finished configuration the RESET-POW-ON pulse will have already finished. So this circuit is for user manual reset but NOT for power up reset.

4.2.1) PUSHB1 , 2 ,3 , 4

All of them are active low. When not pressed a pullup guaranties a high level, when pressed the signal is forced to GND (low level).

IMPORTANT: there are NO provision for debouncing. So the user must supply a debouncing system in his or her FPGA design (or make it inmune to bounces).

pushbutton	signal	FPGA ball name	FPGA ball number
PUSHB1	PUSH_BOT0#	IO_L2P_3	W3
PUSHB2	PUSH_BOT1#	IO_L7N_3	P7
PUSHB3	PUSH_BOT2#	IO_L8P_3	P6
PUSHB4	PUSH_BOT3#	IO_L8N_3	P5

4.3) Microswitches

All of them are active low. When not pressed a pullup guaranties a high level, when pressed the signal is forced to GND (low level).

microswitch position	signal	FPGA ball name	FPGA ball number
1	SWITCH0#	IO_L11P_3	N6
2	SWITCH1#	IO_L11N_3	N7
3	SWITCH2#	IO_L23P_3	M7
4	SWITCH3#	IO_L23N_3	M8

4.4) Testpoints

Some testpoint with hook are provided for easy measurement fo the different power supply voltages.

testpoint	colour	voltage	comment
TP1	Blue	5.0	After proteccion circuits. Will measure 0 volt (or near) if one of the protections is tripped
TP2	Orange	3.3	Fixed 3.3 volt
TP3	Yellow	VCC_CUST	Custom voltage, depends on JMP22 configuration
TP4	Black	GND	Reference for measurements
TP5	Black	GND	Reference for measurements
TP6	White	VCCO-0	Voltage for bank 0 and asociated user connector
TP7	White	VCCO-1	Voltage for bank 0 and asociated user connector
TP8	White	VCCO-2	Voltage for bank 0 and asociated user connector

4.5) Oscillators

4.5.1) 25 MHz

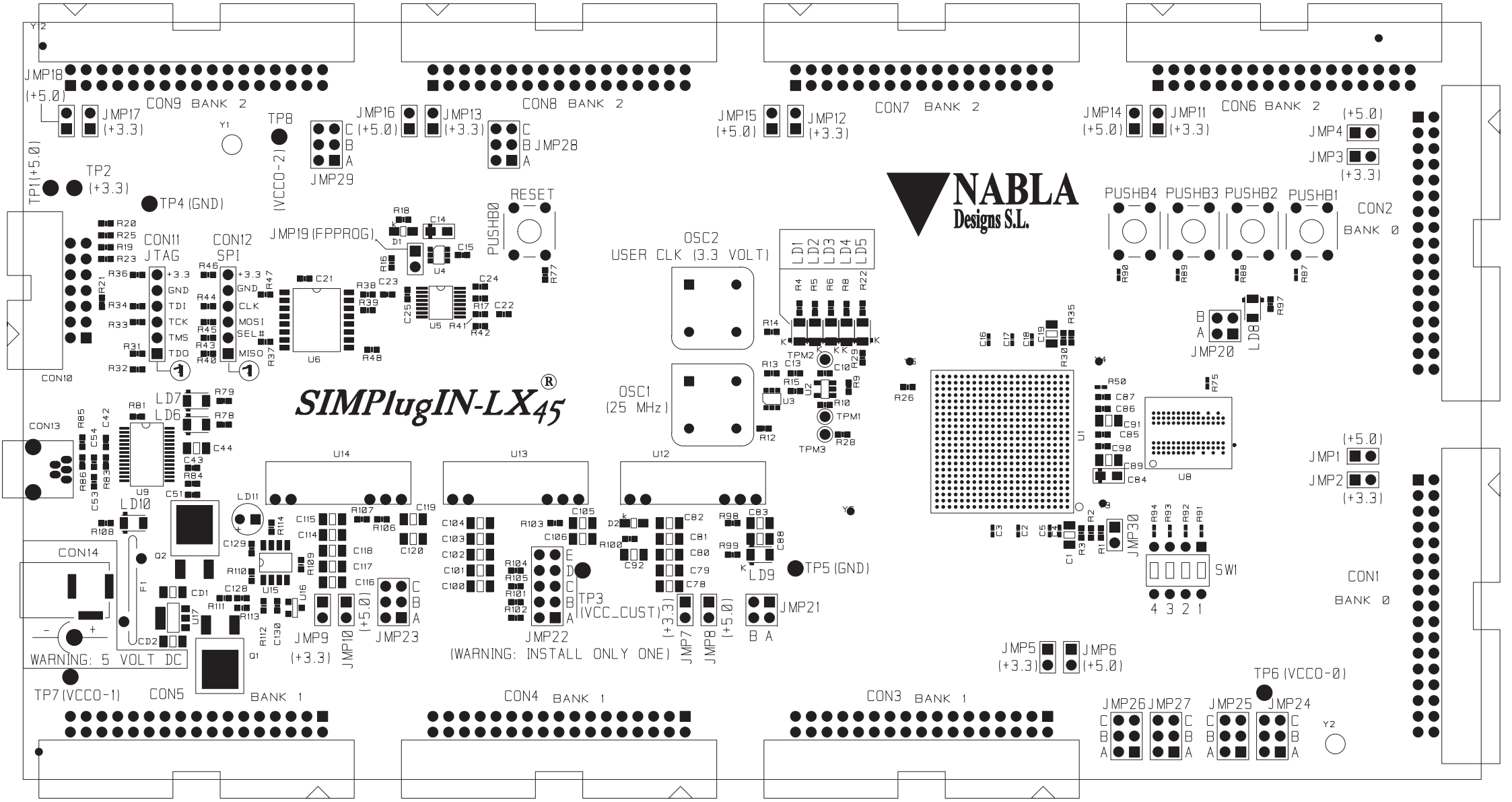
The board is shipped with 25 MHz oscillator installed in OSC1.

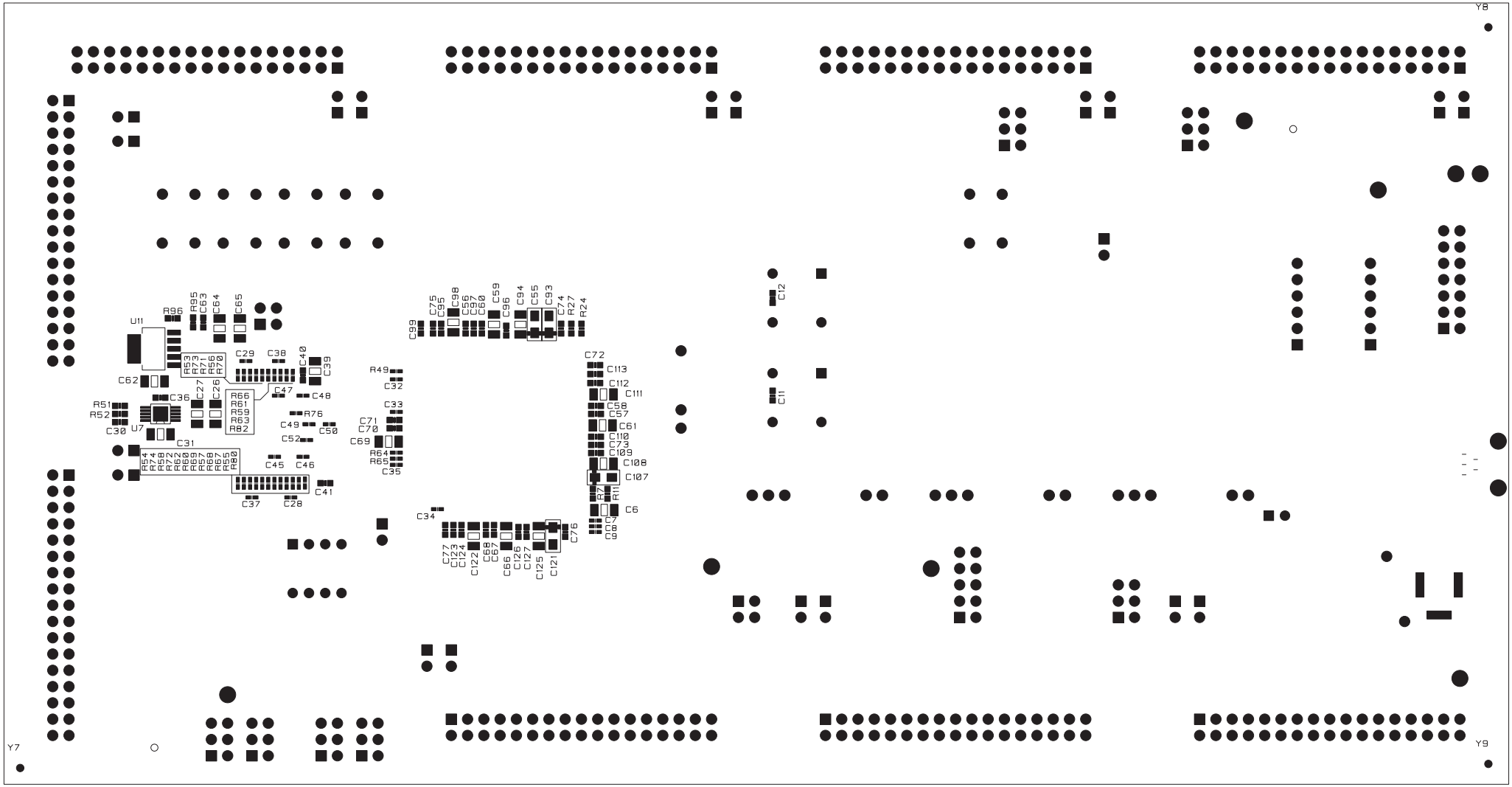
The oscillator is socketed so the user can easily change it (use a 3.3 volt, CMOS, DIP8 oscillator). In that case take into account that some of the examples provided could work in an unexpected way.

4.5.2) User oscillator

There is an empty socket in OSC2. A 3.3 volt, CMOS, DIP8 oscillator should be used.

.


SIMPlugIN-LX45®
NABLA Designs S.L.
CON9 BANK 2
CON8 BANK 2
CON7 BANK 2
CON6 BANK 2
CON5 BANK 1
CON4 BANK 1
CON3 BANK 1
CON2 BANK 0
CON1 BANK 0
CON10
CON11 JTAG
CON12 SPI
CON13
CON14
JMP18 (+5.0)
JMP17 (+3.3)
JMP16 (+5.0)
JMP13 (+3.3)
JMP15 (+5.0)
JMP12 (+3.3)
JMP14 (+5.0)
JMP11 (+3.3)
JMP29
JMP28
JMP19 (FPPROG)
JMP4 (+5.0)
JMP3 (+3.3)
JMP20
JMP1 (+5.0)
JMP2 (+3.3)
JMP30
JMP9 (+3.3)
JMP10 (+5.0)
JMP23
JMP22 (WARNING: INSTALL ONLY ONE)
JMP7 (+3.3)
JMP8 (+5.0)
JMP21
JMP5 (+3.3)
JMP6 (+5.0)
JMP26
JMP27
JMP25
JMP24
TP1 (+5.0)
TP2 (+3.3)
TP3 (VCC_CUST)
TP4 (GND)
TP5 (GND)
TP6 (VCCO-0)
TP7 (VCCO-1)
TP8 (VCCO-2)
RESET
PUSHB0
PUSHB1
PUSHB2
PUSHB3
PUSHB4
OSC1 (25 MHz)
OSC2 USER CLK (3.3 VOLT)
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LD8
LD9
LD10
LD11
SW1
WARNING: 5 VOLT DC
+3.3
GND
TDI
TCK
TMS
TDO
CLK
MOSI
SEL#
MISO


Y8
Y7
Y9
U11
U7
C62
C36
C30
C31
C29
C38
C40
C39
C47
C48
C27
C26
C49
C50
C52
C45
C46
C41
C37
C28
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C72
C113
C112
C111
C58
C57
C61
C110
C73
C109
C108
C107
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C7
C8
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C12
C11
C99
C75
C95
C98
C56
C97
C60
C59
C96
C94
C55
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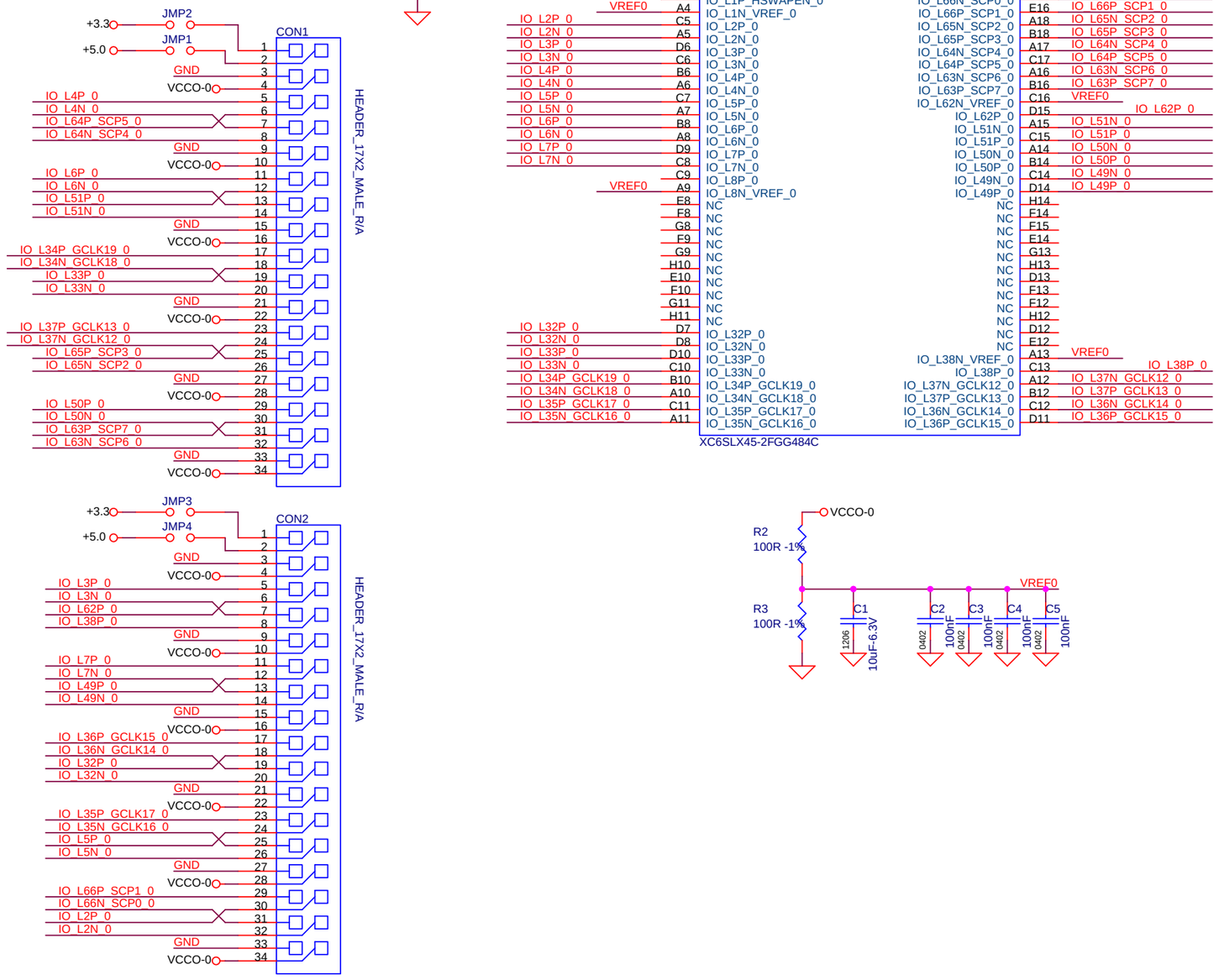
C69
C67
C66
C126
C127
C125
C121



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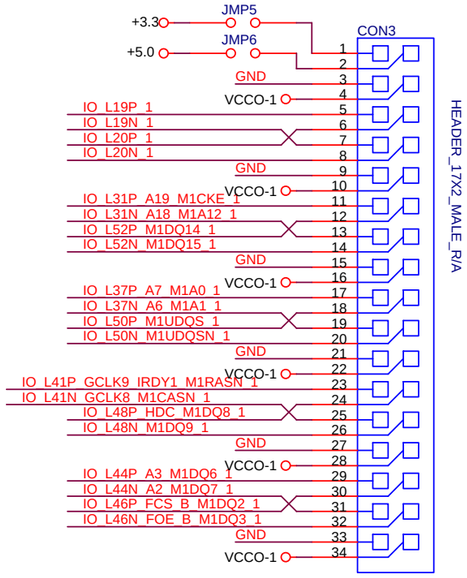
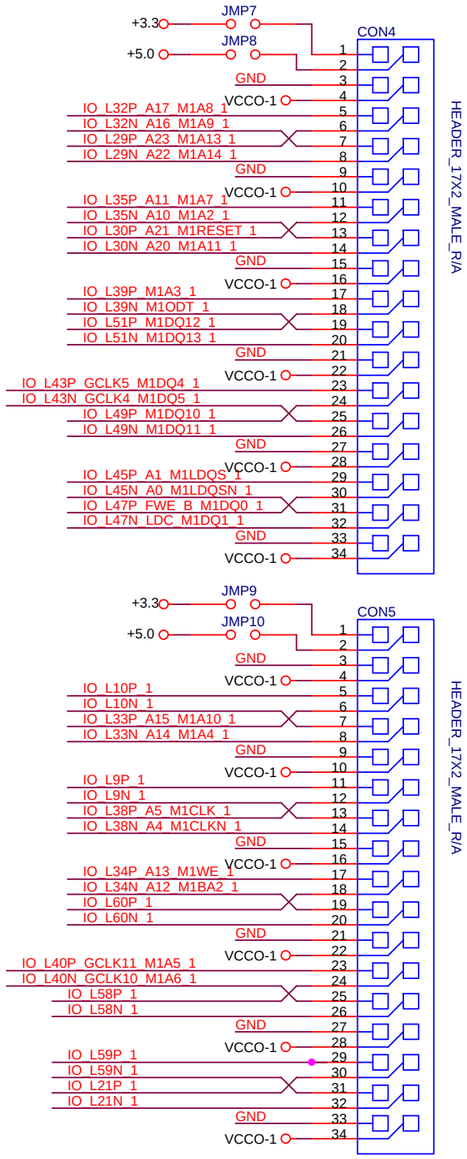
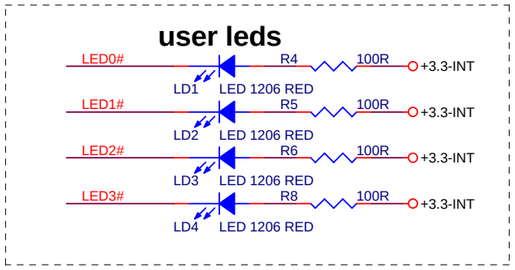
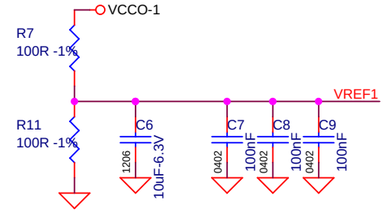
Project: SIMPlugIN	Board: SIMPlugIN-LX45
Board description: Development board, LX45 based	
Size: A3	Page description: FPGA bank 0
Rev 2.3p	
Last modified date: Thursday, August 25, 2011	Page 1 of 5









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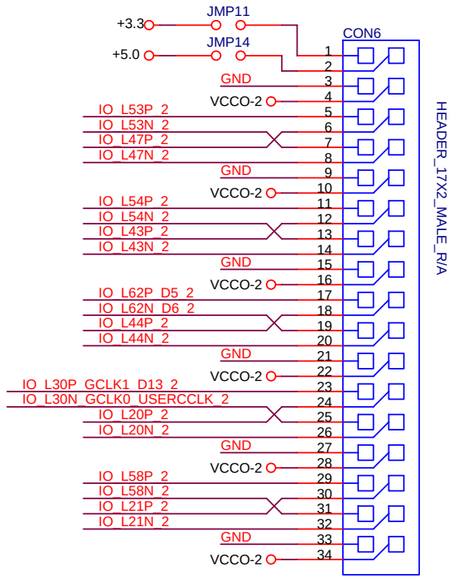
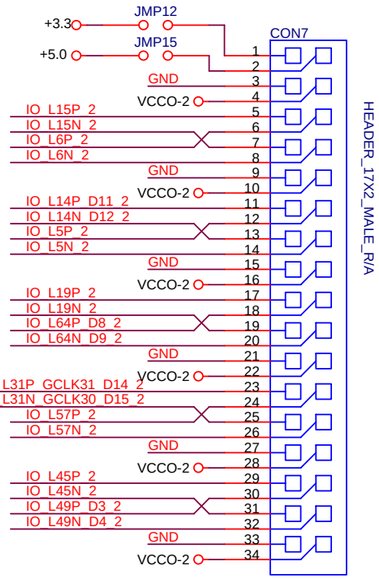
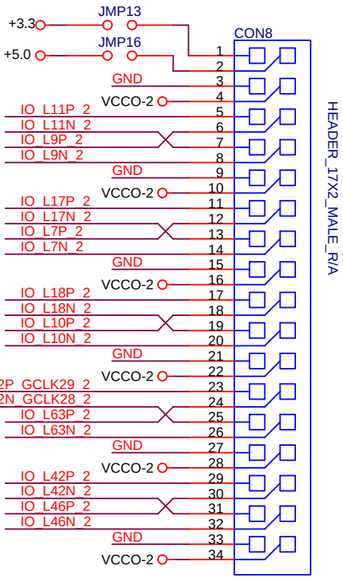
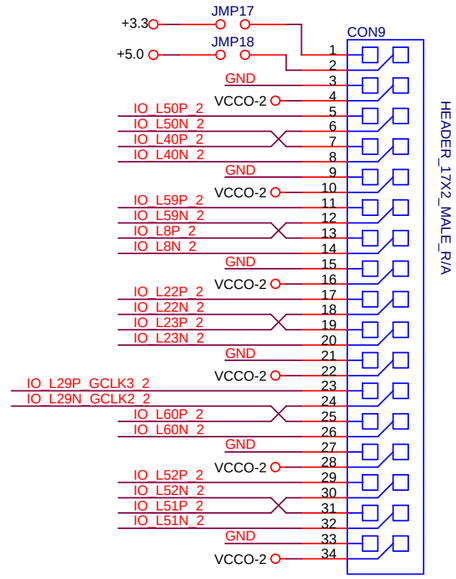
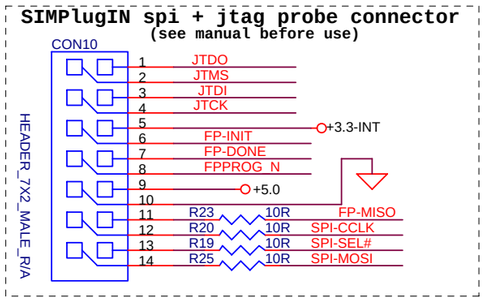
Project: SIMPlugIN	Board: SIMPlugIN-LX45	
Board description: Development board, LX45 based		
Size: A3	Page description: FPGA bank 1 // oscillators , leds	Rev 2.3p
Last modified date: Thursday, August 25, 2011	Page 2 of 5	

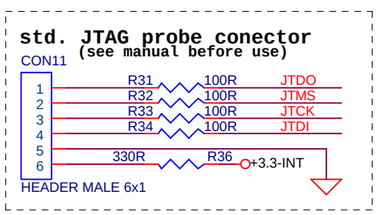


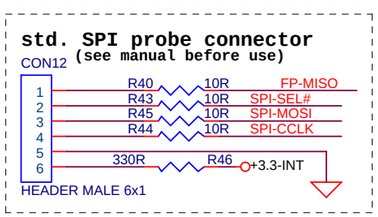


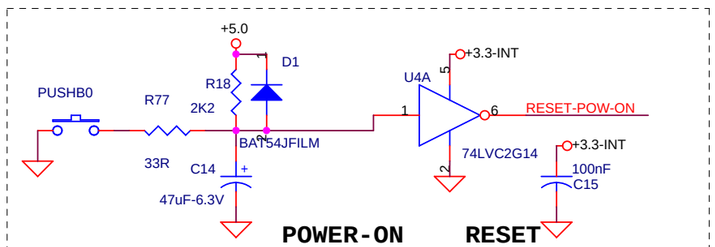


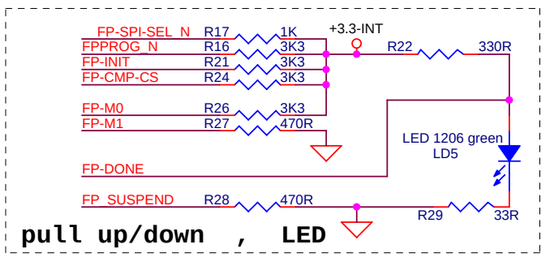


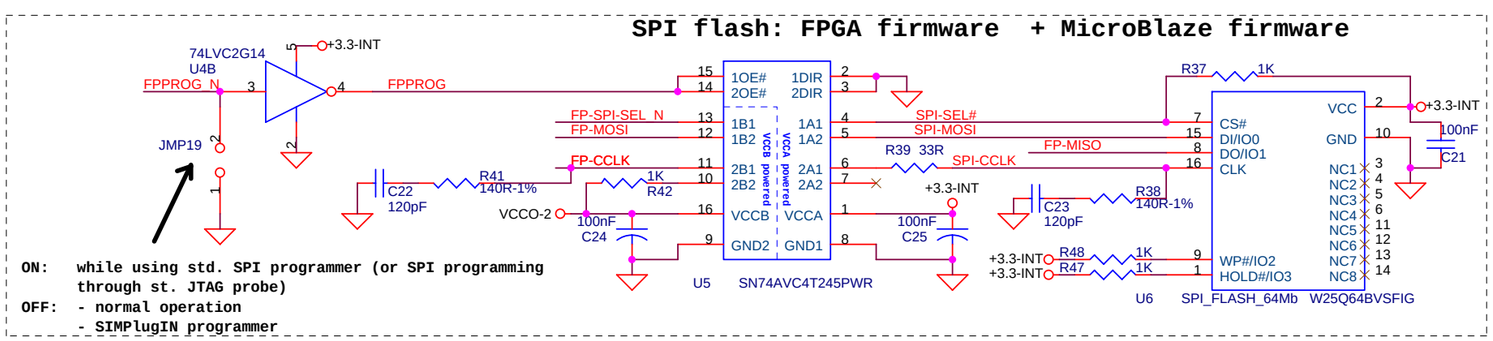


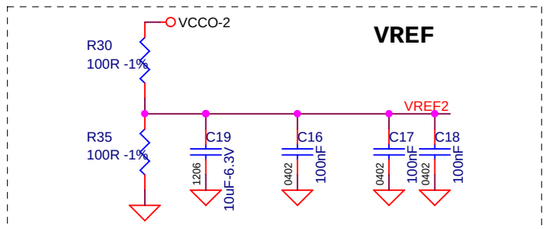












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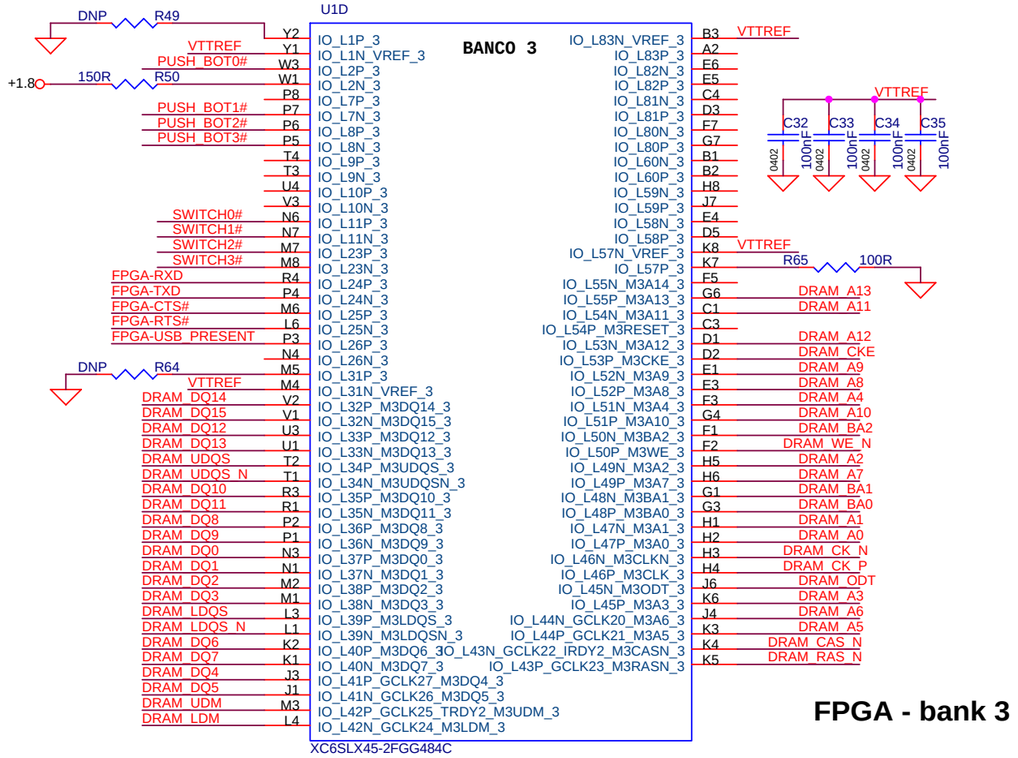
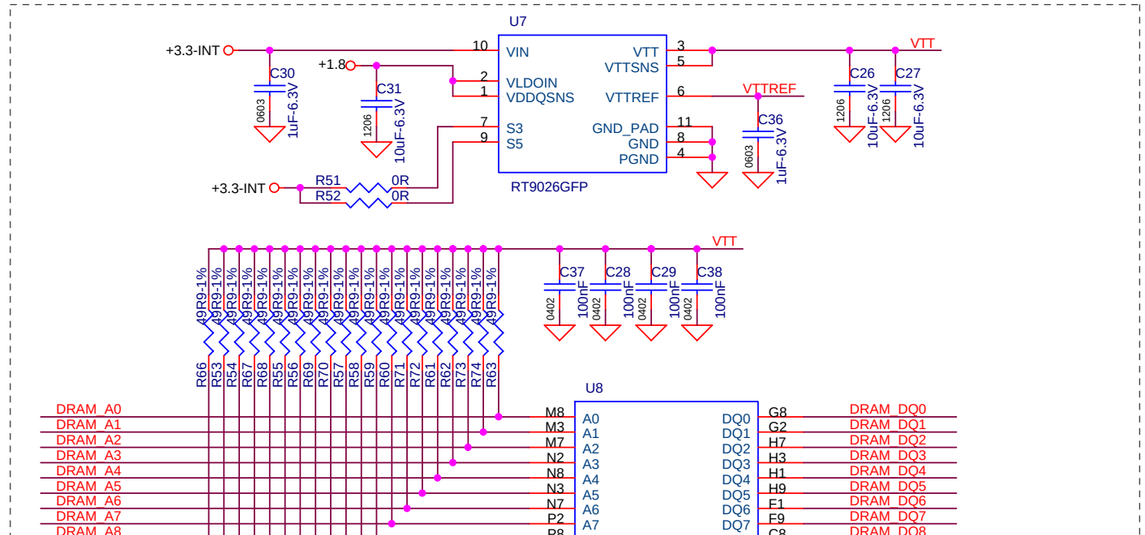
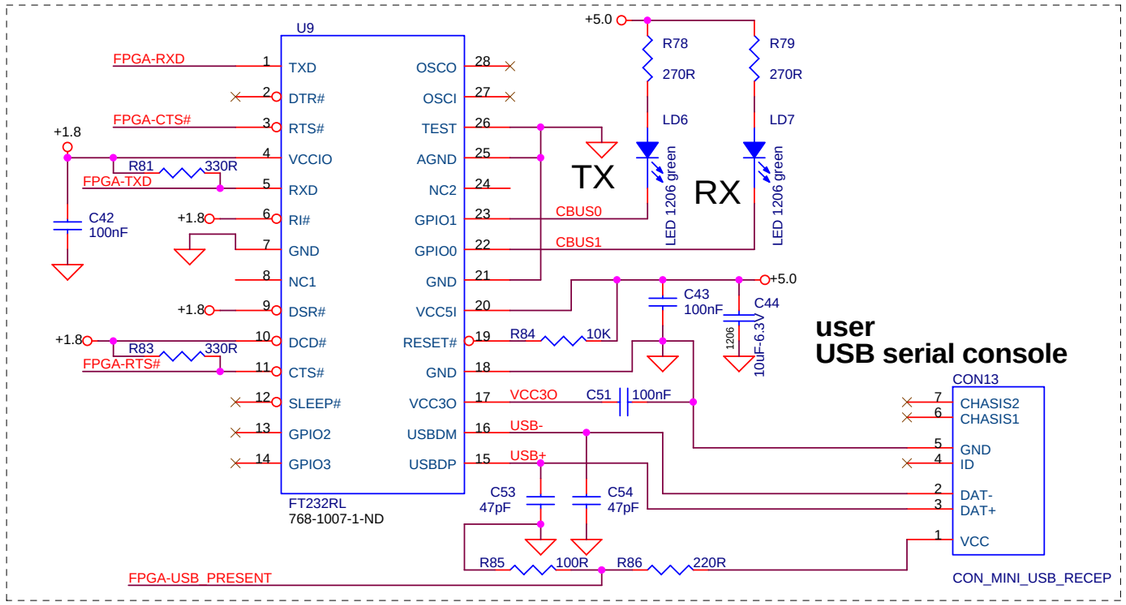
Project: SIMPlugIN	Board: SIMPlugIN-LX45
Board description: Development board, LX45 based	
Size: A3	Page description: FPGA bank 2 // SPI flash memory // programming interface
Rev 2.3p	
Last modified date: Thursday, August 25, 2011	Page 3 of 5



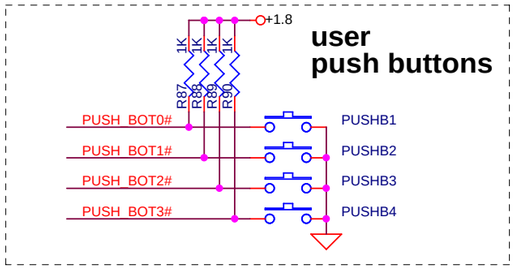
FPGA - bank 3



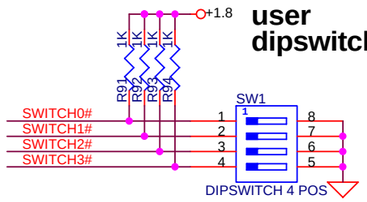
DDR2 memory



user
USB serial console



user
push buttons



user
dipswitch

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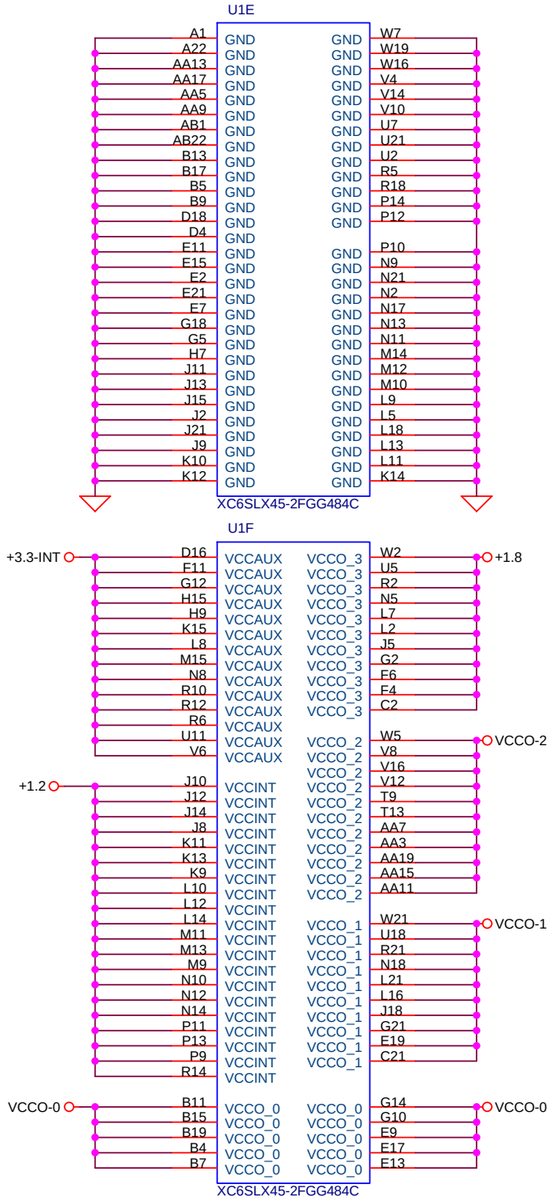
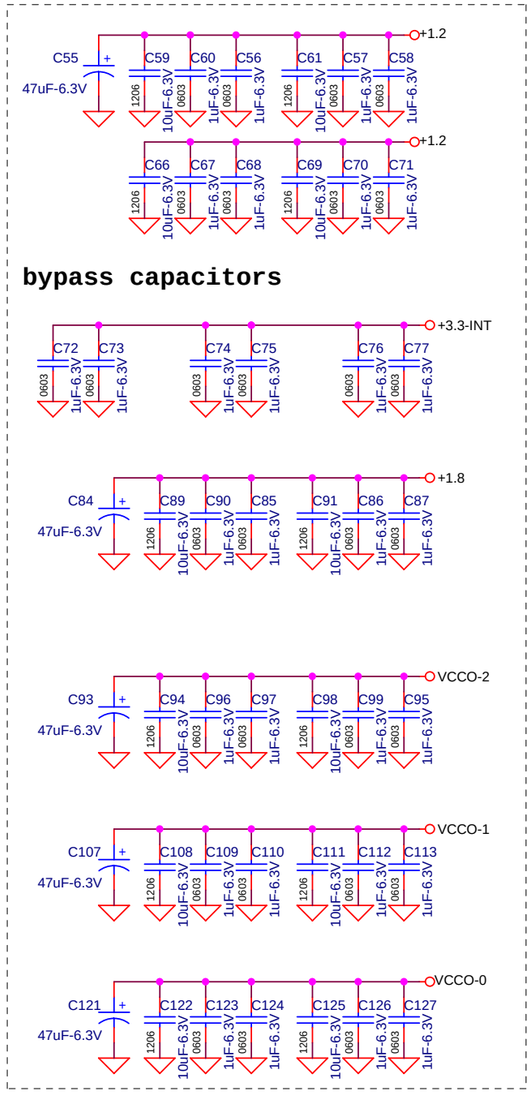
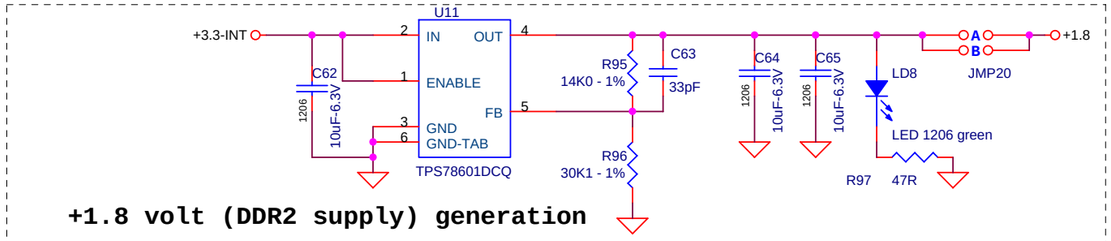
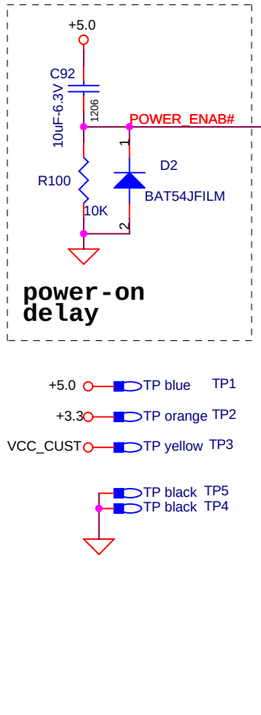
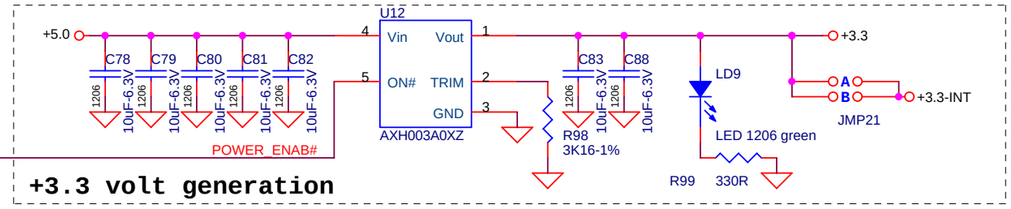
Project: SIMPlugIN	Board: SIMPlugIN-LX45
Board description: Development board, LX45 based	
Size: A3	Page description: FPGA bank 3 // DDR2 // user pushbutton & switches
Rev 2.3p	
Last modified date: Thursday, August 25, 2011	Page 4 of 5

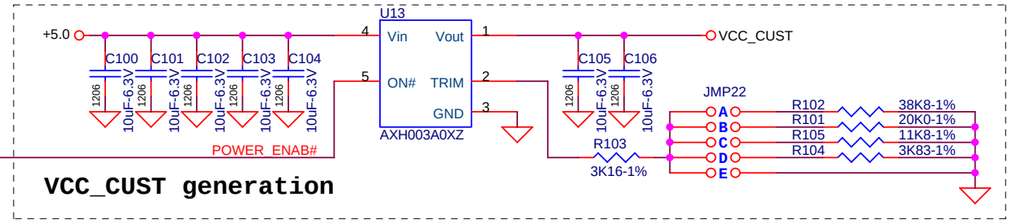


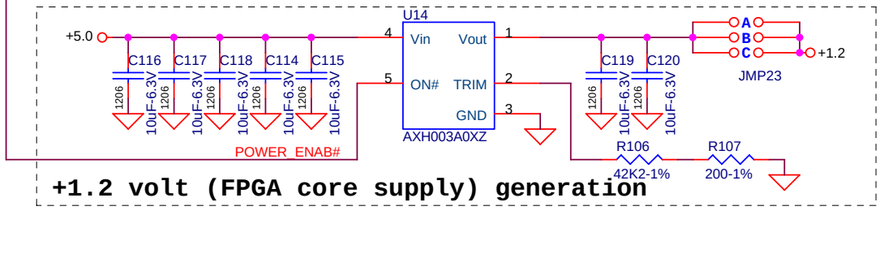


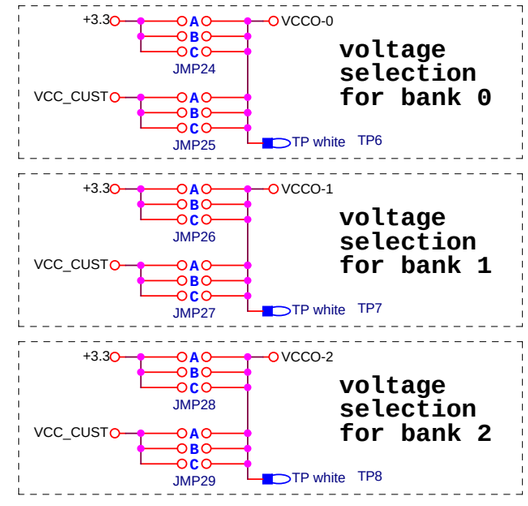


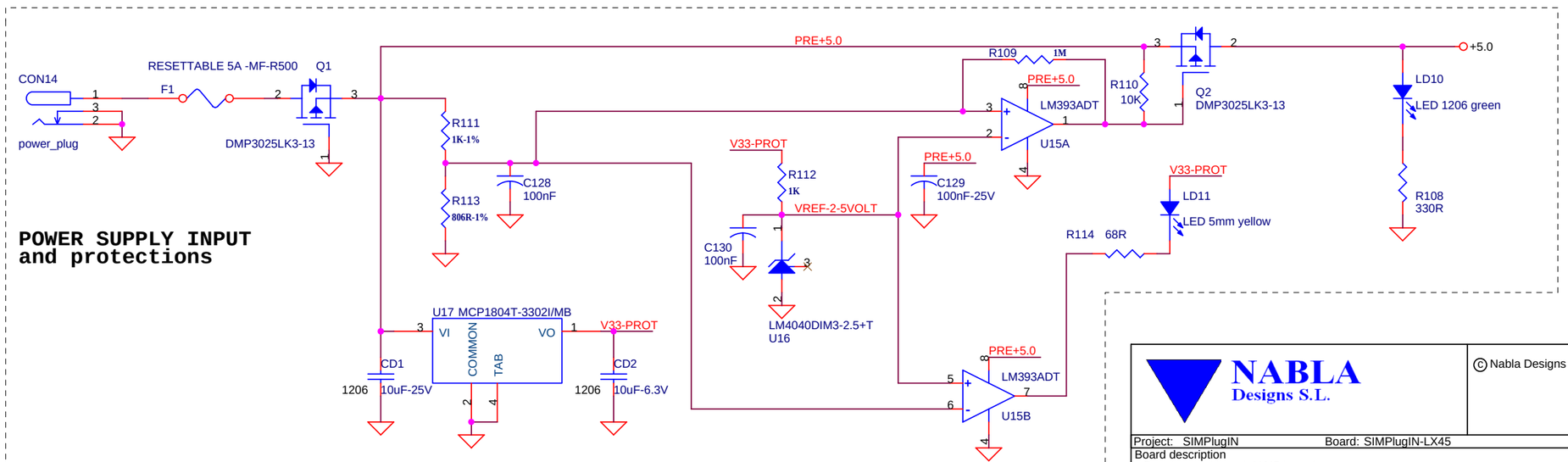












Project: SIMPlugIN	Board: SIMPlugIN-LX45
Board description: Development board, LX45 based	
Size: A3	Page description: power supply
Rev: 2.3p	
Last modified date: Thursday, August 25, 2011	Page 5 of 5

Revised: Thursday, August 25, 2011				
Item	**qty**	**Reference**	**Part**	**PCB footprint**
1	1	CD1	10uF-25V	1206
2	1	CD2	10uF-6.3V	1206
3	9	CON1,CON2,CON3,CON4,CON5,	HEADER_17X2_MALE_R/A	
		CON6,CON7,CON8,CON9		
4	1	CON10	HEADER_7X2_MALE_R/A	
5	2	CON11,CON12	HEADER MALE 6x1	CON6_125
6	1	CON13	CON_MINI_USB_RECEP	
7	1	CON14	power_plug	power_plug
8	45	C1,C6,C19,C26,C27,C31,	10uF-6.3V	1206
		C39,C44,C59,C61,C62,C64,		
		C65,C66,C69,C78,C79,C80,		
		C81,C82,C83,C88,C89,C91,		
		C92,C94,C98,C100,C101,		
		C102,C103,C104,C105,C106,		
		C108,C111,C114,C115,C116,		
		C117,C118,C119,C120,C122,		
		C125		
9	25	C2,C3,C4,C5,C7,C8,C9,C16,	100nF	0402
		C17,C18,C28,C29,C32,C33,		
		C34,C35,C37,C38,C45,C46,		
		C47,C48,C49,C50,C52		
10	13	C10,C11,C12,C13,C15,C21,	100nF	0603
		C24,C25,C42,C43,C51,C128,		
		C130		
11	6	C14,C55,C84,C93,C107,	47uF-6.3V	1206
		C121		
12	2	C22,C23	120pF	0603
13	34	C30,C36,C40,C41,C56,C57,	1uF-6.3V	0603
		C58,C60,C67,C68,C70,C71,		
		C72,C73,C74,C75,C76,C77,		
		C85,C86,C87,C90,C95,C96,		
		C97,C99,C109,C110,C112,		
		C113,C123,C124,C126,C127		
14	2	C54,C53	47pF	0603
15	1	C63	33pF	0603
16	1	C129	100nF-25V	0603
17	2	D2,D1	BAT54JFILM	SOD323
18	1	F1	RESETTABLE 5A -MF-R500	MF-R500
19	20	JMP1,JMP2,JMP3,JMP4,JMP5,	JUMPER_2X1	JUMPER 2 X 1
		JMP6,JMP7,JMP8,JMP9,		
		JMP10,JMP11,JMP12,JMP13,		

		JMP14,JMP15,JMP16,JMP17,		
		JMP18,JMP19,JMP30		
20	2	JMP21,JMP20	JUMPER_2X2	JUMPER 2 X 2
21	1	JMP22	JUMPER_5X2	JUMPER 5 X 2
22	7	JMP23,JMP24,JMP25,JMP26,	JUMPER_3X2	JUMPER 3 X 2
		JMP27,JMP28,JMP29		
23	4	LD1,LD2,LD3,LD4	LED 1206 RED	1206
24	6	LD5,LD6,LD7,LD8,LD9,LD10	LED 1206 green	1206
25	1	LD11	LED 5mm yellow	RADIAL 5mm
26	1	OSC1	25MHz- 3.3 VOLT	OSC8
27	1	OSC2	optional user MHz- 3.3 VOLT	OSC8
28	5	PUSHB1,PUSHB2,PUSHB3,	SWITCH TACTILE 6x6 mm vertical	switch 6x6mm vertical
		PUSHB4,PUSHB0		
29	2	Q1,Q2	DMP3025LK3-13	TO252-3L
30	10	R1,R4,R5,R6,R8,R31,R32,	100R	0603
		R33,R34,R85		
31	6	R2,R3,R7,R11,R30,R35	100R -1%	0603
32	6	R9,R10,R16,R21,R24,R26	3K3	0603
33	7	R12,R13,R14,R15,R29,R39,	33R	0603
		R77		
34	6	R17,R37,R42,R47,R48,R112	1K	0603
35	1	R18	2K2	0603
36	8	R19,R20,R23,R25,R40,R43,	10R	0603
		R44,R45		
37	7	R22,R36,R46,R81,R83,R99,	330R	0603
		R108		
38	2	R28,R27	470R	0603
39	2	R38,R41	140R-1%	0603
40	2	R64,R49	DNP	0402
41	1	R50	150R	0402
42	2	R51,R52	0R	0603
43	20	R53,R54,R55,R56,R57,R58,	49R9-1%	0402
		R59,R60,R61,R62,R63,R66,		
		R67,R68,R69,R70,R71,R72,		
		R73,R74		
44	3	R65,R75,R76	100R	0402
45	2	R79,R78	270R	0603
46	2	R80,R82	4K7	0402
47	3	R84,R100,R110	10K	0603
48	1	R86	220R	0603
49	8	R87,R88,R89,R90,R91,R92,	1K	0402
		R93,R94		

50	1	R95	14K0 - 1%	0603
51	1	R96	30K1 - 1%	0603
52	1	R97	47R	0603
53	2	R103,R98	3K16-1%	0603
54	1	R101	20K0-1%	0603
55	1	R102	38K8-1%	0603
56	1	R104	3K83-1%	0603
57	1	R105	11K8-1%	0603
58	1	R106	42K2-1%	0603
59	1	R107	200-1%	0603
60	1	R109	1M	0603
61	1	R111	1K-1%	0603
62	1	R113	806R-1%	0603
63	1	R114	68R	0603
64	2	SOC1,SOC2	OSCILLATOR SOCKET	DIP 8 OSCILLATOR SOCKET
65	1	SW1	DIPSWITCH 4 POS	SWITCHDIP4
66	3	TPM1,TPM2,TPM3	DNP header 1x1	header 1x1
67	1	TP1	TP blue	keystone tp mp 5011
68	1	TP2	TP orange	keystone tp mp 5011
69	1	TP3	TP yellow	keystone tp mp 5011
70	2	TP5,TP4	TP black	keystone tp mp 5011
71	3	TP6,TP7,TP8	TP white	keystone tp mp 5011
72	1	U1	XC6SLX45-2FGG484C	FG484
73	1	U2	24AA02E48T-I/OT	SOT23_5
74	2	U4,U3	74LVC2G14	SOT23-6
75	1	U5	SN74AVC4T245PWR	TSSOP16
76	1	U6	SPI_FLASH_64Mb W25Q64BVSFIG	SOIC16 - 300MIL
77	1	U7	RT9026GFP	RT9026GFP MSOP10 con pad
78	1	U8	DDR2 64Mx16: W971GG6JB-25	DDR2 x16
79	1	U9	FT232RL	SSOP28
80	1	U11	TPS78601DCQ	SOT223_6
81	3	U12,U13,U14	AXH003A0XZ	AXH003A0XZ
82	1	U15	LM393ADT	SOIC8
83	1	U16	LM4040DIM3-2.5	SOT23
84	1	U17	MCP1804T-3302I/MB	SOT-89-3